

# Jca  
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Form PTO-1449  LIST OF PATENTS AND PUBLICATIONS FOR INFORMATION DISCLOSURE STATEMENT (Use Several Sheets if Necessary)	APPLICANT: Michael Dibrino	
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**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,694,350	Dec.2,'97	Wolrich et al.	364	788	Jun.30,'95
	AB	5,212,662	May 18,'93	Cocanougher et al.	364	748	Sep.11,'90
	AC	4,999,802	Mar.12,'91	Cocanougher et al.	364	748	Jan.13,'85
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

**FOREIGN PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE (#43)	COUNTRY	CLASS	SUBCLASS
	AL					
	AM					
	AN					
	AO					
	AP					

**OTHER INFORMATION (Including Author, Title, Date, Pertinent Pages, Etc.)**

	AR	R.K. Montoye et al., "Design of the IBM RISC System/6000 floating-point execution unit", IBM J. Res. Develop., Vol.34, No. 1, January 1990, pgs. 59-70.
	AS	David R. Lutz et al., "Comparison of two's complement numbers", 1996 Taylor & Francis Ltd., Int. J. Electronics, 1996, Vol. 80, No. 4, pgs. 513-523.
	AT	Stuart F. Oberman et al., "The SNAP Project: Design of Floating Point Arithmetic Units", 1997 IEEE Computer Society, Proceedings of 13 <sup>th</sup> Symposium on Computer Arithmetic, pgs. 156-165.
	AU	M.J. Flynn et al., "The SNAP Project: Towards Sub-Nanosecond Arithmetic", 1995 IEEE, Proceedings on 12 <sup>th</sup> Symposium on Computer Arithmetic, pgs. 75-82.
	AV	Brett Olsson et al., "RISC System/6000 Floating-Point Unit, IBM RISC System/6000 Technology, 1990, pgs. 35-42.
	AW	A.Beaumont-Smith et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures", 1999 IEEE, 14 <sup>th</sup> IEEE Symposium on Computer Arithmetic, 14-16 April 1999, pgs. 35-42.
	AX	
	AY	
	AZ	

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.